

**U74CBTLV3253****CMOS IC****LOW-VOLTAGE DUAL 1-OF-4
FET
MULTIPLEXER/DEMULTIPLEXER****DESCRIPTION**

The **U74CBTLV3253** device is a dual 1-of-4 high-speed FET multiplexer and demultiplexer. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S0, S1) inputs control the data flow. The FET multiplexers/demultiplexers are disabled when the associated output-enable ($\overline{OE}$) input is high.

FEATURES

- * 5Ω Switch Connection Between Two Ports
- * Rail-to-Rail Switching on Data I/O Ports

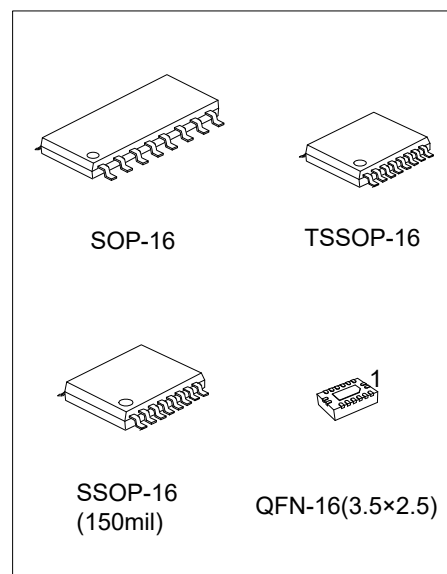
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBTLV3253L-S16-R	U74CBTLV3253G-S16-R	SOP-16	Tape Reel
U74CBTLV3253L-R16-R	U74CBTLV3253G-R16-R	SSOP-16	Tape Reel
U74CBTLV3253L-P16-R	U74CBTLV3253G-P16-R	TSSOP-16	Tape Reel
U74CBTLV3253L-QAH-R	U74CBTLV3253G-QAH-R	QFN-16(3.5×2.5)	Tape Reel

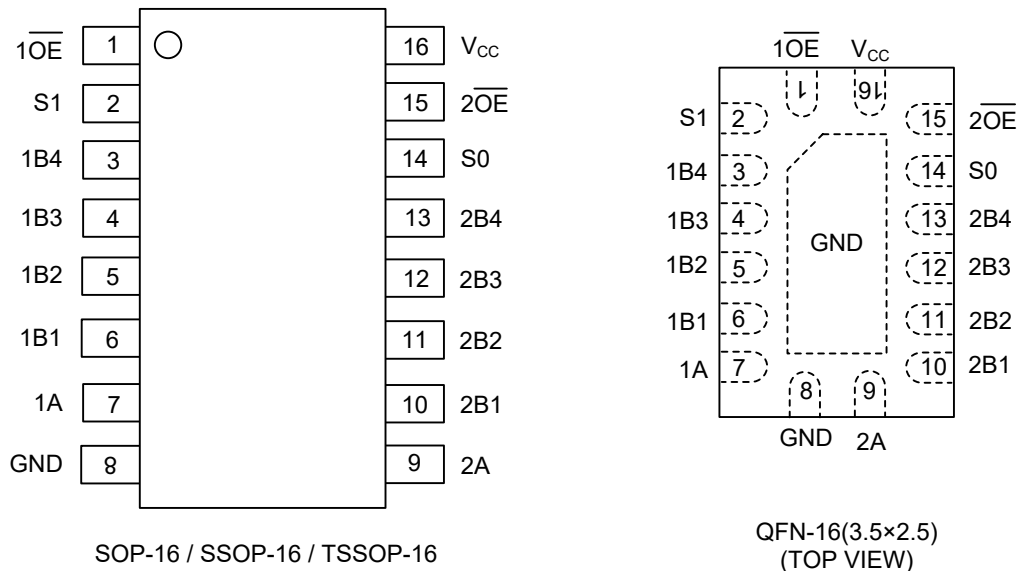
U74CBTLV3253G-S16-R (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube, R: Tape Reel (2) S16: SOP-16, R16: SSOP-16, P16: TSSOP-16 QAH: QFN-16(3.5×2.5) (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

SOP-16 / SSOP-16 / TSSOP-16	QFN-16(3.5×2.5)
16 15 14 13 12 11 10 9 UTC ☐☐☐☐ LV3253 ☐ ☐☐ 1 2 3 4 5 6 7 8 → Date Code L: Lead Free G: Halogen Free → Lot Code	UTC LV 3 2 5 3 ☐ ● ☐☐☐☐☐ → L: Lead Free G: Halogen Free → Date Code ← Lot Code



PIN CONFIGURATION



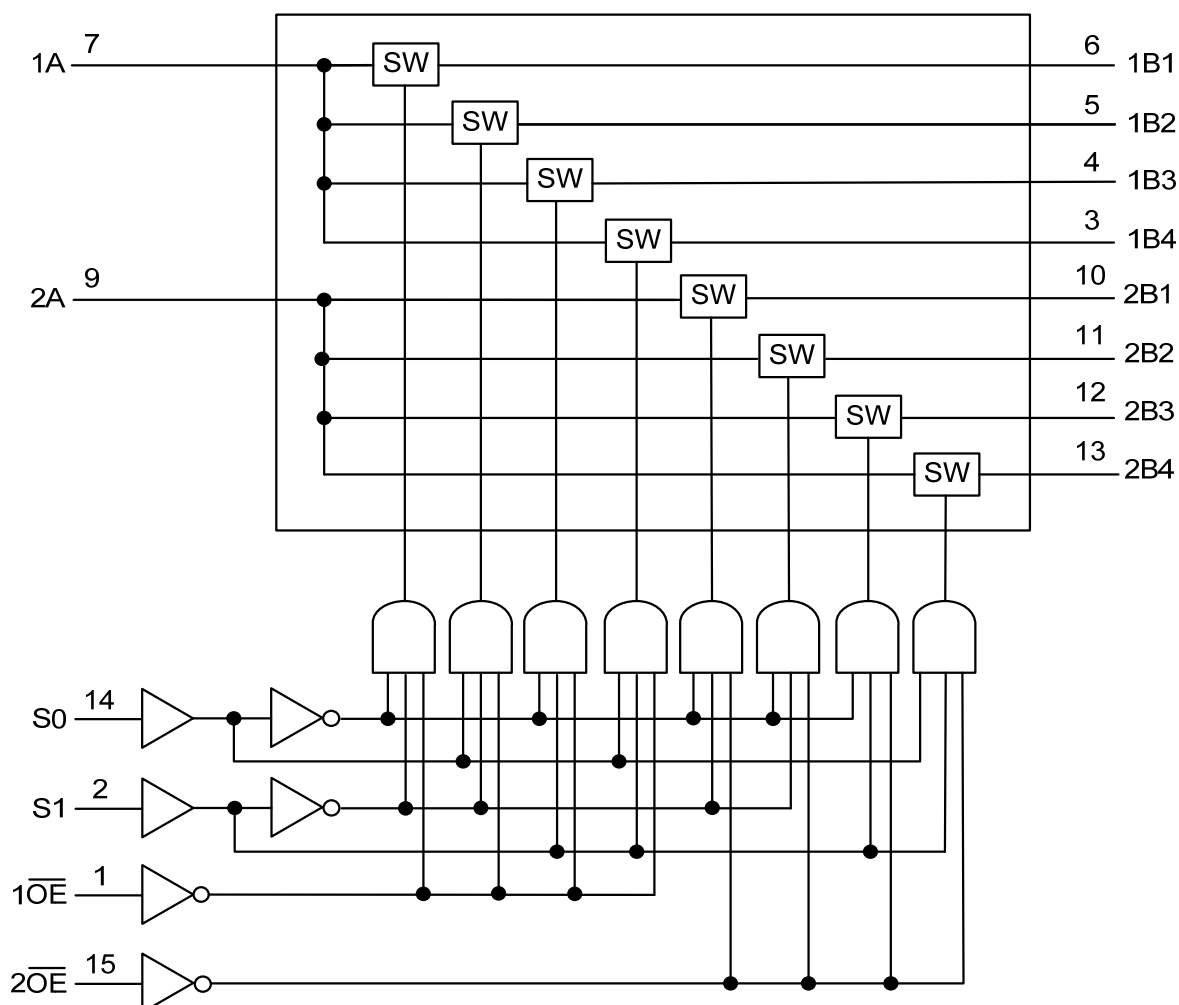
PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	1OE	I	Output Enable 1 Active-Low
2	S1	I	Select Pin 1
3	1B4	I/O	I/O Channel 1 I/O 4
4	1B3	I/O	I/O Channel 1 I/O 3
5	1B2	I/O	I/O Channel 1 I/O 2
6	1B1	I/O	I/O Channel 1 I/O 1
7	1A	I/O	Channel 1 common
8	GND		Ground
9	2A	I/O	Channel 2 common
10	2B1	I/O	Channel 2 I/O 1
11	2B2	I/O	Channel 2 I/O 2
12	2B3	I/O	Channel 2 I/O 3
13	2B4	I/O	Channel 2 I/O 4
14	S0	I	Select Pin 0
15	2OE	I	Output Enable 2 Active-Low
16	V _{CC}		Power

FUNCTION TABLE (Each Multiplexer / Demultiplexer)

INPUTS			FUNCTION
OE	S1	S0	
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

■ **LOGIC DIAGRAM** (positive logic)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 4.6	V
Input Voltage (Note 2)	V_{IN}		-0.5 ~ 4.6	V
Switch I/O Voltage (Note 2)	$V_{I/O}$		-0.5 ~ 4.6	V
Continuous Channel Through V_{CC} or GND			±128	mA
Input Clamp Current	I_{IK}	$V_{IN} < 0$	-50	mA
I/O Port Clamp Current	$I_{I/OK}$	$V_{IO} < 0$	-50	mA
Junction Temperature	T_J		+150	°C
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	90	°C/W
	SSOP-16	120	°C/W
	TSSOP-16	115	°C/W
	QFN-16(3.5×2.5)	135	°C/W

■ RECOMMENDED OPERATING CONDITIONS

(Over operating free-air temperature range, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.3		3.6	V
High-control input voltage	V_{IH}	$V_{CC}=2.3V \sim 2.7V$	1.7			V
		$V_{CC}=2.7V \sim 3.6V$	2			V
Low-control input voltage	V_{IL}	$V_{CC}=2.3V \sim 2.7V$			0.7	V
		$V_{CC}=2.7V \sim 3.6V$			0.8	V
Operating Temperature	T_A		-40		+125	°C

Note: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^{\circ}C$			$T_A=-40^{\circ}C \sim +125^{\circ}C$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Digital Input Diode Voltage	V_{IK}	$V_{CC}=3V, I_I=-18mA$			-1.2			-1.2	V
Input Leakage Current	I_I	$V_{CC}=3.6V, V_I=V_{CC}$ or GND			±1			±20	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=3.6V, V_I=V_{CC}$ or GND, $I_O=0$			10			50	μA
Additional Quiescent Supply Current (Note 1)	Control Inputs	ΔI_{CC}			300			2000	μA
Resistor Between Two Ports (Note 2)	R_{ON}	$V_{CC}=2.3V$							
		TYP at $V_I=0$							
		$I_I=64mA$		5	8			15	Ω
		$I_I=24mA$		5	8			15	Ω
		$V_{CC}=2.5V$							
		$V_I=1.7V$		27	40			60	Ω
	R_{ON}	$V_{CC}=3V$							
		$V_I=0V$							
		$I_I=64mA$		5	7			11	Ω
		$I_I=24mA$		5	7			11	Ω
	R_{ON}	$V_I=2.4V$							
		$I_I=15mA$		10	15			26	Ω

Notes: 1. This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

2. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

■ SWITCHING CHARACTERISTICS

See Fig. 1 and Fig. 2 for test circuit and waveforms.

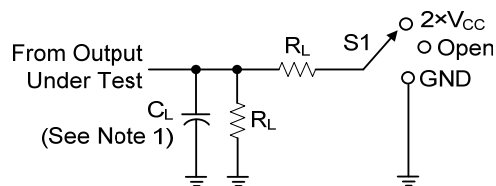
PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay From Input (A or B) (Note) to Output (B or A)	t _{pd} (t _{PLH} /t _{PHL})	V _{CC} =2.5V±0.2V			0.15			0.3	ns
		V _{CC} =3.3V±0.3V			0.25			0.5	ns
Propagation Delay From Input (S) to Output (A or B)	t _{pd} (t _{PLH} /t _{PHL})	V _{CC} =2.5V±0.2V	1		7.3			8.8	ns
		V _{CC} =3.3V±0.3V	1		6.8			8.3	ns
Propagation Delay From Input (S) to Output (A or B)	t _{en} (t _{PZL} /t _{PZH})	V _{CC} =2.5V±0.2V	1		7.3			9.3	ns
		V _{CC} =3.3V±0.3V	1		7			9	ns
Propagation Delay From Input ($\overline{\text{OE}}$) to Output (A or B)	t _{en} (t _{PZL} /t _{PZH})	V _{CC} =2.5V±0.2V	1		6.5			8.5	ns
		V _{CC} =3.3V±0.3V	1		6.3			8.3	ns
Propagation Delay From Input (S) to Output (A or B)	t _{dis} (t _{PLZ} /t _{PHZ})	V _{CC} =2.5V±0.2V	1		7.1			9.1	ns
		V _{CC} =3.3V±0.3V	1		7.5			9.5	ns
Propagation Delay From Input ($\overline{\text{OE}}$) to Output (A or B)	t _{dis} (t _{PLZ} /t _{PHZ})	V _{CC} =2.5V±0.2V	1		6.5			8.5	ns
		V _{CC} =3.3V±0.3V	1		6.4			8.4	ns

Note: The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

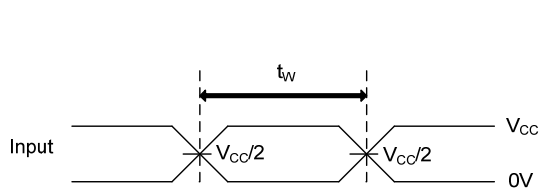
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Control Input Capacitance	Control Inputs	C _i	V _O =3V or 0		3		pF
I/O Capacitance (OFF)	A Port	C _{IO(OFF)}	V _O =3V or 0, $\overline{\text{OE}}$ =V _{CC}		20.5		pF
	B Port				5.5		pF

■ TEST CIRCUIT AND WAVEFORMS

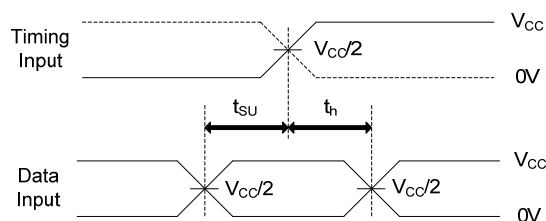


V_{CC}	C_L	R_L	V_{Δ}
$2.5V \pm 0.2V$	30pF	500Ω	0.15V
$3.3V \pm 0.3V$	50pF	500Ω	0.3V

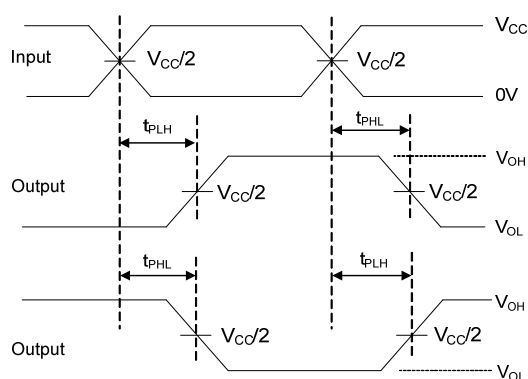
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



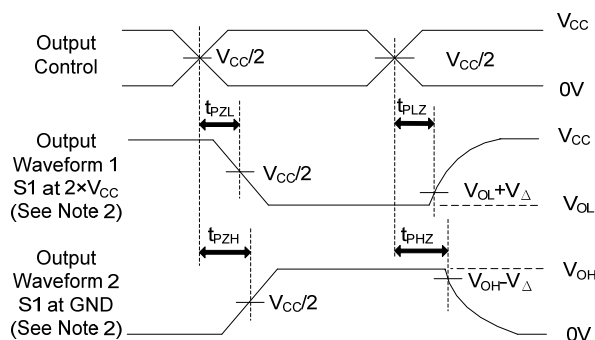
PULSE DURATION



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

3. All input pulses are supplied by generators having the following characteristics:

$P_{RR} \leq 10\text{MHz}$, $Z_0 = 50\Omega$, $t_r \leq 2\text{ns}$, $t_f \leq 2\text{ns}$.

4. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

5. t_{PZL} and t_{PZH} are the same as t_{en} .

6. t_{PLH} and t_{PHL} are the same as t_{pd} .

Load circuitry and voltage waveforms

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