



ULN62064

LINEAR INTEGRATED CIRCUIT

PRECISION MICROPOWER SHUNT VOLTAGE REFERENCE

DESCRIPTION

The UTC **ULN62064** is high-voltage, high-current darlington drivers comprised of four NPN darlington pairs.

All units feature integral clamp diodes for switching inductive loads.

For proper operation, the substrate (SUB) must be connected to the most negative voltage.

Applications include relay, hammer, lamp and stepping motor drivers.

FEATURES

- * Output current (single output): 1.5A (Max.)
- * High sustaining voltage output: 50V (Min.)
- * Output clamp diodes
- * Input compatible with TTL and 5V CMOS

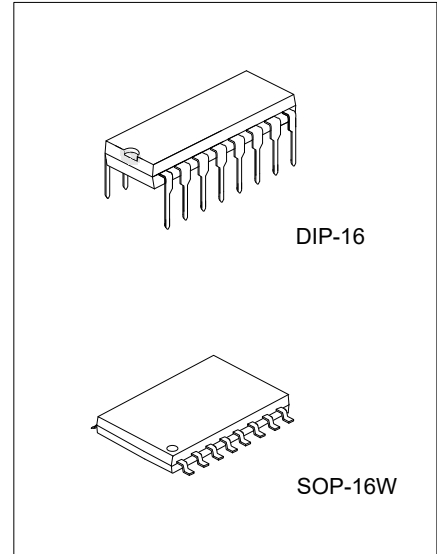
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULN62064L-D16-T	ULN62064G-D16-T	DIP-16	Tube
ULN62064L-S16W-T	ULN62064G-S16W-T	SOP-16W	Tube
ULN62064L-S16W-R	ULN62064G-S16W-R	SOP-16W	Tape Reel

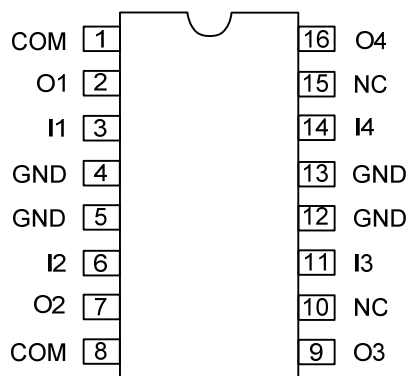
ULN62064G-D16-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube, R: Tape Reel (2) D16: DIP-16, S16W: SOP-16W (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

DIP-16	SOP-16W
16 15 14 13 12 11 10 9 UTC □□□□ ULN62064 □ □□ 1 2 3 4 5 6 7 8 Date Code L: Lead Free G: Halogen Free Lot Code	16 15 14 13 12 11 10 9 UTC □□□□ ULN62064 □ □□ 1 2 3 4 5 6 7 8 Date Code L: Lead Free G: Halogen Free Lot Code



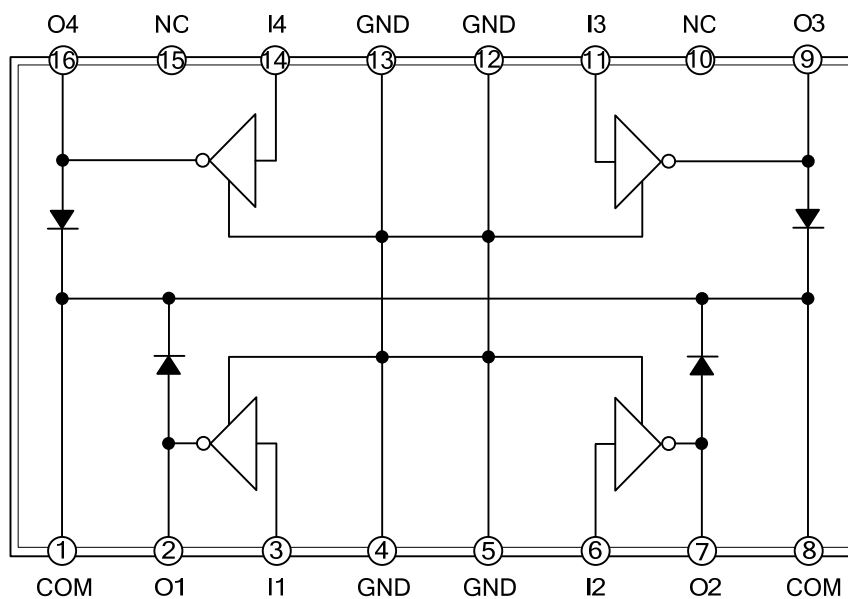
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	COM	Common pin
2	O1	Output pin 1
3	I1	Input pin 1
4	GND	GND pin
5	GND	GND pin
6	I2	Input pin 2
7	O2	Output pin 2
8	COM	Common pin
9	O3	Output pin 3
10	NC	Non-connection pin
11	I3	Input pin 3
12	GND	GND pin
13	GND	GND pin
14	I4	Input pin 4
15	NC	Non-connection pin
16	O4	Output pin 4

BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless other specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Output Sustaining Voltage		V _{CE (SUS)}	-0.5 ~ 50	V
Output Current		I _{OUT}	1.5	A/ch
Input Current		I _{IN}	50	mA
Input Voltage		V _{IN}	-0.5 ~ 17	V
Clamp Diode Reverse Voltage		V _R	50	V
Clamp Diode Forward Current		I _F	1.5	A
Power Dissipation	DIP-16	P _D	1.47 / 2.7 (Note 2)	W
	SOP-16W		0.75 / 1.25 (Note 2)	W
Operating Temperature		T _{OPR}	-40 ~ +85	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. On Glass Epoxy PCB (50 × 50 × 1.6 mm Cu 50%).

■ OPERATING RANGES (T_A= -40 ~ +85°C, unless other specified)

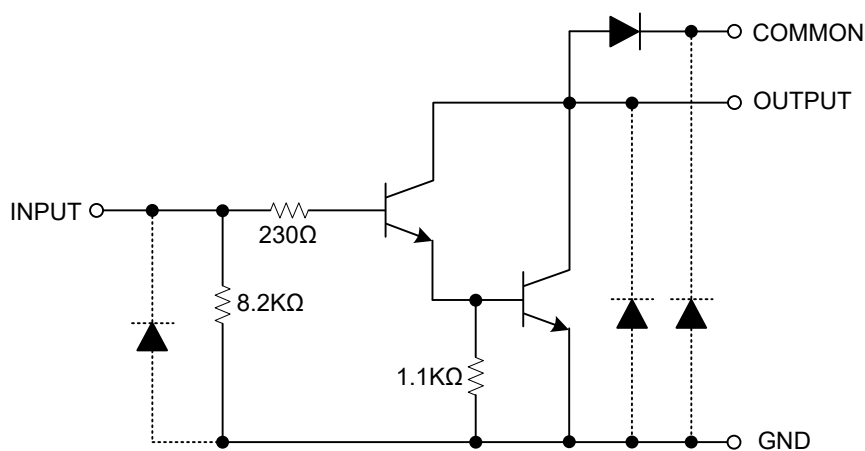
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Sustaining Voltage	V _{CE (SUS)}		0		50	V
Output Current (Note)	I _{OUT}	DC1 Circuit, T _A =25°C	0		1250	mA/ch
		tpw = 25ms	0		1250	mA/ch
		4 Circuits	0		390	mA/ch
		T _A = 85°C	0		830	mA/ch
		T _J = 120°C	0		160	mA/ch
Input Voltage	V _{IN}		0		8	V
Input Voltage (Output On)	V _{IN (ON)}	I _{OUT} = 1.25A	2.5		8	V
Input Voltage (Output Off)	V _{IN (OFF)}		0		0.4	V
Input Current	I _{IN}		0		20	mA
Clamp Diode Reverse Voltage	V _R		0		50	V
Clamp Diode Forward Current	I _F				1.25	A
Power Dissipation	DIP-16	P _D	T _A = 85°C (Note 1)		1.4	W
	SOP-16W		T _A = 85°C (Note 1)		0.65	W

Note: On Glass Epoxy PCB (50 × 50 × 1.6 mm Cu 50%).

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless other specified)

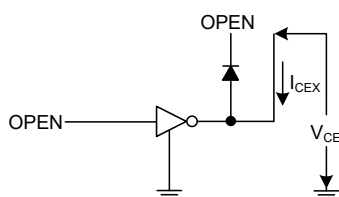
PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Leakage Current	I _{CEX}	1	V _{CE} =50V, T _A =25°C			50	μA
			V _{CE} =50V, T _A =85°C			500	μA
Collector-Emitter Saturation Voltage	V _{CE (sat)}	2	I _{OUT} =1.25A, I _{IN} =2mA			1.6	V
			I _{OUT} =0.75A, I _{IN} =935μA			1.25	V
DC Current Transfer Ratio	h _{FE}	2	V _{CE} =2V		2500		
			I _{OUT} =1.0A		3000		
			I _{OUT} =1.25A				
Input Voltage (Output On)	V _{IN (ON)}	3	I _{OUT} =1.25A, I _{IN} =2mA			2.4	V
Clamp Diode Leakage Current	I _R	4	V _R =50V, T _A =25°C			50	μA
			V _R =50V, T _A =85°C			100	μA
Clamp Diode Forward Voltage	V _F	5	I _F =1.25A			2	V
Input Capacitance	C _{IN}	6			15		pF
Turn-On Delay	t _{ON}	7	C _L =15pF, V _{OUT} =50V, R _L =42Ω		0.1		μs
Turn-Off Delay	t _{OFF}	7	C _L =15pF, V _{OUT} =50V, R _L =42Ω		1.0		μs

■ SCHEMATICS (EACH DRIVER)

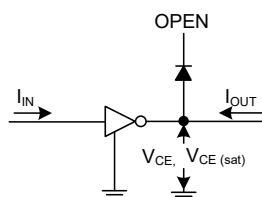


■ TEST CIRCUIT

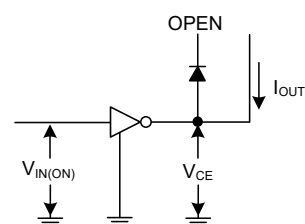
1. I_{CEX}



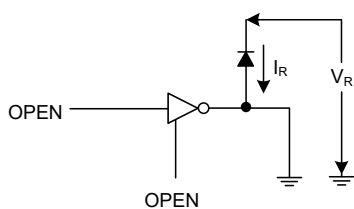
2. $V_{CE(sat)}$, h_{FE}



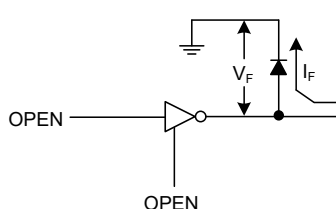
3. $V_{IN(ON)}$



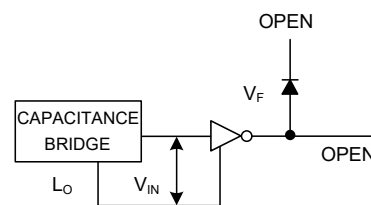
4. I_R



5. V_F

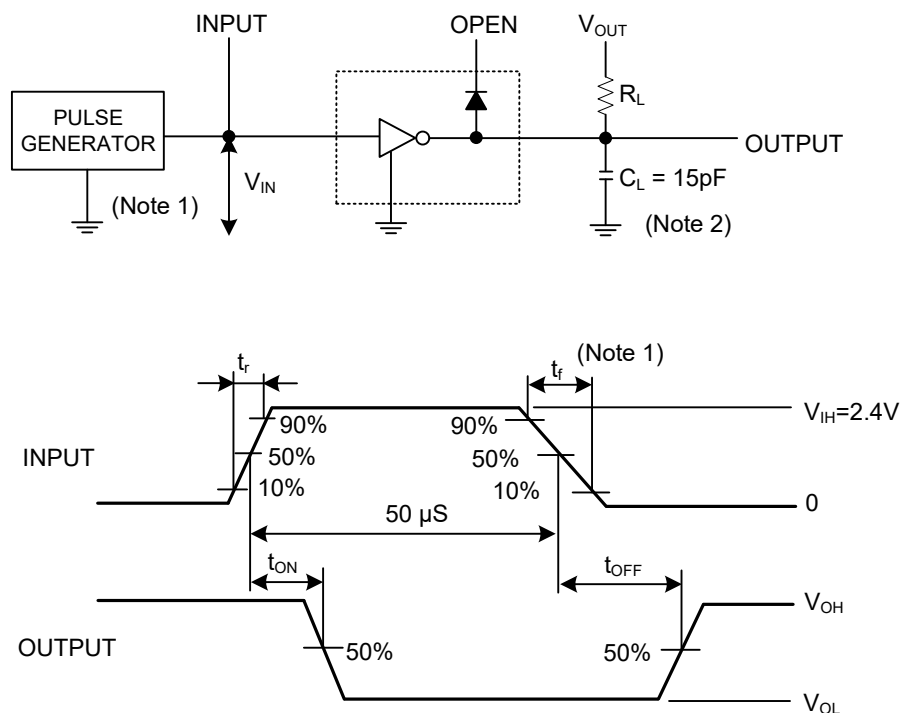


6. C_{IN}



■ TEST CIRCUIT

7. t_{ON} , t_{OFF}



Notes 1: Pulse Width $50 \mu s$, Duty Cycle 10%
 Output Impedance 50Ω , $t_r \leq 5ns$, $t_f \leq 10ns$
 2: C_L includes probe and jig capacitance.

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